Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] What is claimed is:

1.A processing system electrically connected to a computer, the processing system comprising:
a non-volatile memory (NVM) for storing firmware needed by the processing system; and
an NVM control interface having a plurality of registers for updating and reading data stored in the NVM;
wherein when the NVM control interface updates a current piece of data stored in the NVM, the NVM control interface first reads a prior piece of data that is stored in the NVM prior to the current piece of data and transmits the prior piece of data to the computer for comparison, then the NVM control interface updates the current piece of data.

[c2] 2. The processing system of claim 1 further comprising a processor for controlling operations of the processing system and a bus controller electrically connected to the processor, the NVM, and the NVM control interface for controlling data transmission between the processor, the NVM, and the NVM control interface.

[c3] 3. The processing system of claim 2 wherein the proces-

sor is capable of loading the firmware from the NVM via the bus controller.

[c4] 4. The processing system of claim 1 further comprising a serial port interface electrically connected between the computer system and the NVM control interface for converting serial data bits received from the computer into data bytes and for converting data bytes received from the NVM control interface into serial data bits.

[c5] 5. The processing system of claim 4 wherein a serial port of the serial port interface is a RS-232 (Recommended Standard-232) port.

[c6] 6. The processing system of claim 1 wherein before the NVM control interface reads the prior piece of data, the NVM control interface verifies that the prior piece of data has been written into the NVM.

[c7] 7. The processing system of claim 1 wherein the NVM is a flash read-only memory (flash ROM).

[c8] 8. The processing system of claim 1 wherein the NVM control interface comprises:
an NVM address register for setting addresses of the NVM, wherein an address stored in NVM address register is increased after a write/read (W/R) operation of the NVM is finished;

an NVM page register for setting a download capacity of the NVM;

an NVM data register for storing a data byte stored in the address set by the NVM address register;

a plurality of control bits for setting an operational mode of the NVM; and

a plurality of command registers for executing commands so as to control operations of the NVM.

[c9] 9. The processing system of claim 1 wherein during the update of the firmware stored in the NVM, no data access between the processor and the NVM is allowed.

[c10] 10. A method for updating a firmware stored in a non-volatile memory (NVM) of a processing system, the processing system being electrically connected to a computer system and further comprising a NVM control interface having a plurality of registers for updating and accessing data stored in the NVM, the method comprising:

using the NVM control interface to update a current piece of data stored in the NVM; and

during the update of the current piece of data, using the NVM control interface to read a prior piece of data that is stored in the NVM prior to the current piece of data and transmitting the prior piece of data to the computer for comparison, then updating the current piece of data.

[c11] 11. The method of claim 10 wherein the processing system further comprises a processor for controlling operations of the processing system and a bus controller electrically connected to the processor, the NVM, and the NVM control interface for controlling datatransmission between the processor, the NVM, and the NVM control interface.

[c12] 12. The method of claim 11 wherein the processor is capable of loading the firmware stored in the NVM via the bus controller.

[c13] 13. The method of claim 10 wherein the processing system further comprises a serial port interface electrically connected between the computer system and the NVM control interface for converting serial data bits received from the computer into data bytes and for converting data bytes received from the NVM control interface into serial data bits.

[c14] 14. The method of claim 13 wherein a serial port of the serial port interface is a RS-232 (Recommended Standard-232) port.

[c15] 15. The method of claim 10 further comprising:
verifying that the prior piece of data has been written into the NVM before the NVM control interface reads the

prior piece of data.

[c16] 16. The method of claim 10 wherein the NVM is a flash read-only memory (flash ROM).

[c17] 17. The method of claim 10 wherein the NVM control interface comprises:
an NVM address register for setting addresses of the NVM, wherein an address stored in NVM address register is increased after a write/read (W/R) operation of the NVM is finished;
an NVM page register for setting a download capacity of the NVM;
an NVM data register for storing a data byte stored in the address set by the NVM address register;
a plurality of control bits for setting operation mode of the NVM; and
a plurality of command registers for executing commands so as to control operations of the NVM.

[c18] 18. The method of claim 10 further comprising:
forbidding any data access between the processor and the NVM during the update of the firmware stored in the NVM.